

Final Program



December 6-7, 2006
The Westin Los Angeles Airport
Los Angeles, California

Wednesday, December 6, 2006

7:00 Registration/Continental Breakfast

8:00 **Welcome and Opening Remarks**

Ronald Lacoce, Workshop Chair, The Aerospace Corporation
Yuan Chen, Technical Program Chair, JPL

8:25 **Keynote Presentation I**

Microelectronics Qualification Challenges for Robotic Space Missions
Richard Brace, Chief Project Assurance Manager, JPL

Session I: Reliability Challenges for Advanced Technologies

Session Chair: *Harald Schone, Jet Propulsion Laboratory*

9:25 Reliability Assessment for New Technologies: Advanced Transistor Gate Stacks
Gennadi Bersuker, Sematech

9:50 Break

10:20 Characterizing Negative Bias Temperature Instability in Advanced Gate Dielectrics
John Suehle, NIST

10:45 Copper / Low k Dielectric Interconnects: Integration and Reliability
Glenn Alers, Novellus Systems

11:10 SiC pn-gated Field Effect Transistor for Extreme Temperatures
Mike Mazzola, SemiSouth

11:35 Packaging for High Speed Digital Electronics
Andrew Shapiro, JPL

12:00 Conference Luncheon

Final Program



December 6-7, 2006
The Westin Los Angeles Airport
Los Angeles, California

Wednesday, December 6, 2006 (cont.)

Session II: Memory and ESD

Session Chair: Don Mayer, Aerospace

- 1:40 A Manufacturable and Embeddable Non-Volatile Memory for High Temperature and High Reliability Applications – Development and Characterization Information
Mammen Thomas and Jagdish Pathak, MEMTEK, LLC
- 2:05 ESD Tester Issues from a Design Engineering Standpoint
E. Worley, Silicon Crossing, Inc

Session III: Radiation Effects on Microelectronics

Session Chair: Dave Alexander, Air Force Research Laboratories

- 2:30 Modeling Single Event Effects in Advanced CMOS Processes
Jeff Black, Vanderbilt University
- 2:55 Break
- 3:25 Radiation-enabled Predictive Technology Modeling Approaches for Deep-submicron CMOS IC Design
Hugh Barnaby, Arizona State University
- 3:50 Prospects for Ultra-low Power Radiation-Hardened by Design VLSI
Larry Clark, Arizona State University
- 4:15 A Technical and Cost Perspective for Radiation Testing Challenges
Ken LaBel, Nasa Goddard SFC
- 5:00 Hosted Reception on-site

Final Program



December 6-7, 2006
The Westin Los Angeles Airport
Los Angeles, California

Thursday, December 7, 2006

7:30 Registration/Continental Breakfast

8:00 Announcements

8:05 **Keynote Presentation II**

Silicon Technology Trends: Reliability Challenges and Opportunities
Jose Maiz, Intel Fellow, Director of Logic Technology Q&R, Intel

9:00 **Panel Discussion:** Advanced Technology Reliability Impact on Product Qualification Methodology
Session Chair: *Yuan Chen, Jet Propulsion Laboratory*

10:25 Break

Session IV: FPGA Applications

Session Chair: *Jon Osborn, Aerospace*

10:55 Application Specific Qualification of FPGAs for Space Application
Doug Sheldon, JPL

11:20 FPGA Conversion to ASIC: Turning Convenience into a More Reliable Product
Terry Danzer, AMIS

11:45 Conference Luncheon

Final Program



December 6-7, 2006
The Westin Los Angeles Airport
Los Angeles, California

Thursday, December 7, 2006 (cont.)

Session V: Product Reliability and Qualification

Session Chair: *Mark White, Jet Propulsion Laboratory*

- 1:35 Medical Device Reliability and Qualification
Mark Porter, Medtronics
- 2:00 The Design and Qualification of DC-DC Converters for Extreme Environments
Harvey Stanley, Interpoint
- 2:25 Reliability Update on the Aeroflex ViaLink™ FPGA
Bob Bauer, Aeroflex
- 2:50 Break

Session VI: Advanced Packaging Technologies

Session Chair: *Reza Ghaffarian, JPL*

- 3:10 Extreme High Temperature Packaging
Pat McCluskey, University of Maryland
- 3:35 Embedded Flip Chip on Flex
Linda Del Castillo, JPL
- 4:00 Electronics and IC Packaging Trends
Reza Ghaffarian, JPL
- 4:25 Closing Remarks