

Technology Update Status on Field Programmable Gate Arrays (FPGAs)

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Agenda Topics

- **Background**
- **FPGA Technologies**
- **New Technology Approach**
- **Insertion Plan Requirements**
- **Status of FPGAs**
 - **Actel**
 - **Xilinx**
- **Summary**

Background

- **In recent years, the government, during acquisition reform, has not required space systems manufacturers to absolutely utilize space-qualified parts in their systems.**
- **Systems manufacturers have evaluated the best part available and determined through a self-selected series of tests and analyses that a specific device is acceptable and meets the system performance and reliability requirements.**
- **However, based on a number of recent problems experienced, which have had a critical impact upon launch schedules as well as on-orbit performance, it has been determined that a more stringent approach to parts, materials and processes must be followed.**

Background

- **Therefore, a review of the space level requirements for utilization was begun.**
- **The government is currently in the process of re-invigorating specs and standards that will be imposed on contract for the space user community**
- **The specs and standards will require the use of a full-up space qualified part**
- **A document (ATR-2005(9308)-1 New PMP Technology Insertion Guidelines) was created to provide a set of guidelines to enable the appropriate insertion of new technologies.**

FPGA Technologies

- **The space contractors have been requesting the supplier base to offer technologies that are QML Class V approved**
- **Two manufacturers of FPGAs have embarked on obtaining QML Class V approval**
 - **Actel Antifuse RTAX Series of FPGAs**
 - **Xilinx SRAM based Virtex family of FPGAs**

New Technology Approach

- **MIL-PRF-38535 revised to include requirements for**
 - **Detailed characterization/evaluation and understanding of physics of failure (including electrical, mechanical, thermal and chemical properties that could contribute to root cause failures throughout the product life cycle)**
 - **Activation energy**
 - **Process and performance margins and their sensitivities**
 - **Process trending**
 - **Yield enhancement**
 - **Failure Modes Effects Analysis to consider each mode of failure to ascertain the effects on device operation and reliability of each failure mode**
 - **Requires the development of a plan and procedures defining the methodology and approach by the integrated circuit manufacturer**
 - **Submittal to DSCC with the required approvals**

Insertion Plan Requirements

- **Characterization**
 - **Activation Energies of the major failure mechanisms**
 - **Process variability analysis**
 - **Wafer Lot Acceptance**
 - **Long Term Reliability Testing and Failure Rates**
- **Manufacturing**
 - **Process must be documented**
 - **System must be established to ensure configuration and control**
 - **Statistical Process Controls must be implemented**
 - **Evaluation of maturity of manufacturing process**
 - **Multiple manufacturing lots**
 - **Process and performance repeatability**
 - **Yield**

Status of FPGAs

Actel

- **Actel obtained QML Q (avionics level) approval from DSCC for RTAX (150 nm) in April 06 in chip/wire and LGA packages**
- **Actel Testing**
 - **120 RTAX2000 parts, 6000 hours, 125C test completed in Aug 2006**
 - **No anti-fuse failures; One failure reported as due to a Silicon-to-metal contact (Tungsten plug)**
 - **Part level testing consistent with requirements of MIL-PRF-38535**
 - **500K hrs of commercial AX family qualification testing (no antifuse failures)**
 - **1.8M hrs of RTAX family qualification testing (no antifuse failures)**
- **Actel submitted a QML Class V plan to DSCC in December 2006**
- **The Aerospace Corporation, NASA and DSCC provided comments**
- **Decision reached that visits to foundry and packaging facility were required**
- **The Aerospace Corporation**
 - **746 AX2000 (commercial pkg) parts, simultaneous antifuse and SRAM tests at 3 temp conditions, >1M accumulated device hours**
 - **No antifuse failures**
 - **Two potential SRAM anomalies under investigation**

Actel RTAX FPGA

- **Under Government sponsorship, The Aerospace Corporation initiated a long-term independent test of the 2 million-gate RTAX2000S FPGA in April 2007 utilizing the commercial version of the part (AX2000 product)**
- **The purpose of the test program**
 - **Independently evaluate the anti-fuse reliability**
 - **Characterize the on-board SRAM memory that is new with the device.**
 - **The goal is to ascertain the FIT rate (failures in time (per 10^9 hrs))**
 - **Develop a FIT rate calculator based on all available The Aerospace Corporation's and Actel data.**

Aerospace Test Program Overview

- The Aerospace Corporation's FPGA reliability test program consists of two tests executed concurrently
- RTAX FPGA Test Program - Antifuse Characterization
- Purpose: Bound the antifuse FIT rate and ensure it supports meeting space program's system level reliability and dependability requirements
- Test Article: Actel AX2000-FG896I
- Duration: 1000 hrs; then convert to long term test
- # of Test Articles: 746
- Conditions
 - Test antifuses in combinational logic and in timing sensitive clock nets
 - Group 1: Elevated temp stressing @ 85 C
 - Group 2: Low temp stressing @ -40 C
 - Group 3: Temp cycling (-40 C to +85 C, 10 min transition time, 30 min dwell time) 100 cycles; take data, perform analysis, then proceed to 1000 cycles
- Pass/Fail Criteria: Delta timing delay that supports meeting the reliability allocation
- Comment: Concurrent DPA (destructive physical analysis) of devices to be performed as necessary. Data logging and time collection performed for all boards whenever powered.

Aerospace Test Program Overview

- **RTAX FPGA Test Program - 2**
- **Test Name: SRAM Functional Test (integrated into and conducted simultaneously with the Antifuse Characterization test)**
- **Purpose: Characterize the long term functional performance of the new on board memory**
- **Test Article: Actel AX2000-FG896I**
- **Duration: 1000 hours; then convert to long term test**
- **# of Test Articles: 746**
- **All conditions, test spans and criteria are the same as Antifuse Characterization test**

The Aerospace Corporation's Test Results

- **At the time of this writing, The Aerospace Corporation's test has accumulated ~ 3.0 million device hours with no known antifuse anomalies**
- **Data verification and analyses are under way. Combining this data set with those from tests conducted at Actel, an antifuse FIT rate can be calculated.**
- **In addition, two SRAM test anomalies have been observed at first observation and are under investigation**
 - **Believe these anomalies would have been screened out as part of extended test flow of RT product**
- **The Aerospace Corporation has developed a FIT rate calculator including antifuses, memory and CMOS**
 - **Will be made available to industry after review with Actel**
- **The Aerospace Corporation performed cross-sectional analysis of antifuses and CMOS structures**
 - **No observable issues with antifuse**
 - **Have observed some metallization voids and working with Actel and foundry to understand**

Actel Status

- **DSCC audit of Taiwan foundry conducted Oct 2007**
 - **No issues observed with foundry**
 - **Areas needing closure with Actel**
 - **Physics of failure**
 - **Activation Energy**
 - **Review of Process Changes – foundry/Actel**
 - **Reliability monitors**
- **Still required to assess and validate Kyocera San Diego assembly facility with DSCC**

Xilinx Status

- Presented an overview to Xilinx in December 2004 of space requirements for new technology
- Meeting held with Xilinx in March 2005 to discuss space requirements
 - Participating space contractors included General Dynamics, Honeywell, JPL, and Lockheed Martin
 - Boeing started to work with Xilinx at a later time period
- Weekly telecons held with Xilinx for 1.5 years starting April 2005 to develop a flow, requirements and documents for hermetic and flip-chip devices
- Started with MIL-PRF-38535 Class V Flow
 - Flip-chip devices had to take into account tests and inspections that do not make sense
 - Flip-chip devices also require tests/inspections that hermetic devices do not require
- Flow also required to account for column grid array packaging

Xilinx Status

- Preliminary flow developed and provided to DSCC
- Xilinx has generated procedures and process documents
- The Aerospace Corporation has reviewed the procedures and process documents
 - Resolved issues and Xilinx modified documents where necessary
- Reviewed requirements for new technology insertion with Xilinx
 - Need to correlate data to technologies 0.25 um, 0.15 um, 90 nm, 65 nm
- Visited foundry in Taiwan with Xilinx and DSCC in Oct 2007
- DSCC audit of Taiwan fab conducted Oct 2007
 - No issues observed with foundry
 - Areas needing closure with Xilinx
 - Physics of failure
 - Activation Energy
 - Review of Process Changes – foundry/Xilinx
 - Reliability monitors
 - Long term reliability (life test) data
- The Aerospace Corporation and Xilinx visited packaging facility in April 2007 and added tests/inspections/reliability monitors to flow
- Still required to assess and validate assembly facility with DSCC
- The Aerospace Corporation has performed cross-sections of Xilinx device and did not observe any anomalies

Summary

- **Space community requirements changing for utilization of new technology insertion**
- **Working with 2 FPGA manufacturers to obtain QML Class V approval**
 - **Plans/tests/data being bounded and coming to closure**
 - **The Aerospace Corporation is performing independent tests and evaluations on technology and product**

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