"standard" qualification procedures/standards in their industry, the challenges and future directions

2006 MQRW: panel discussion

J. Maiz

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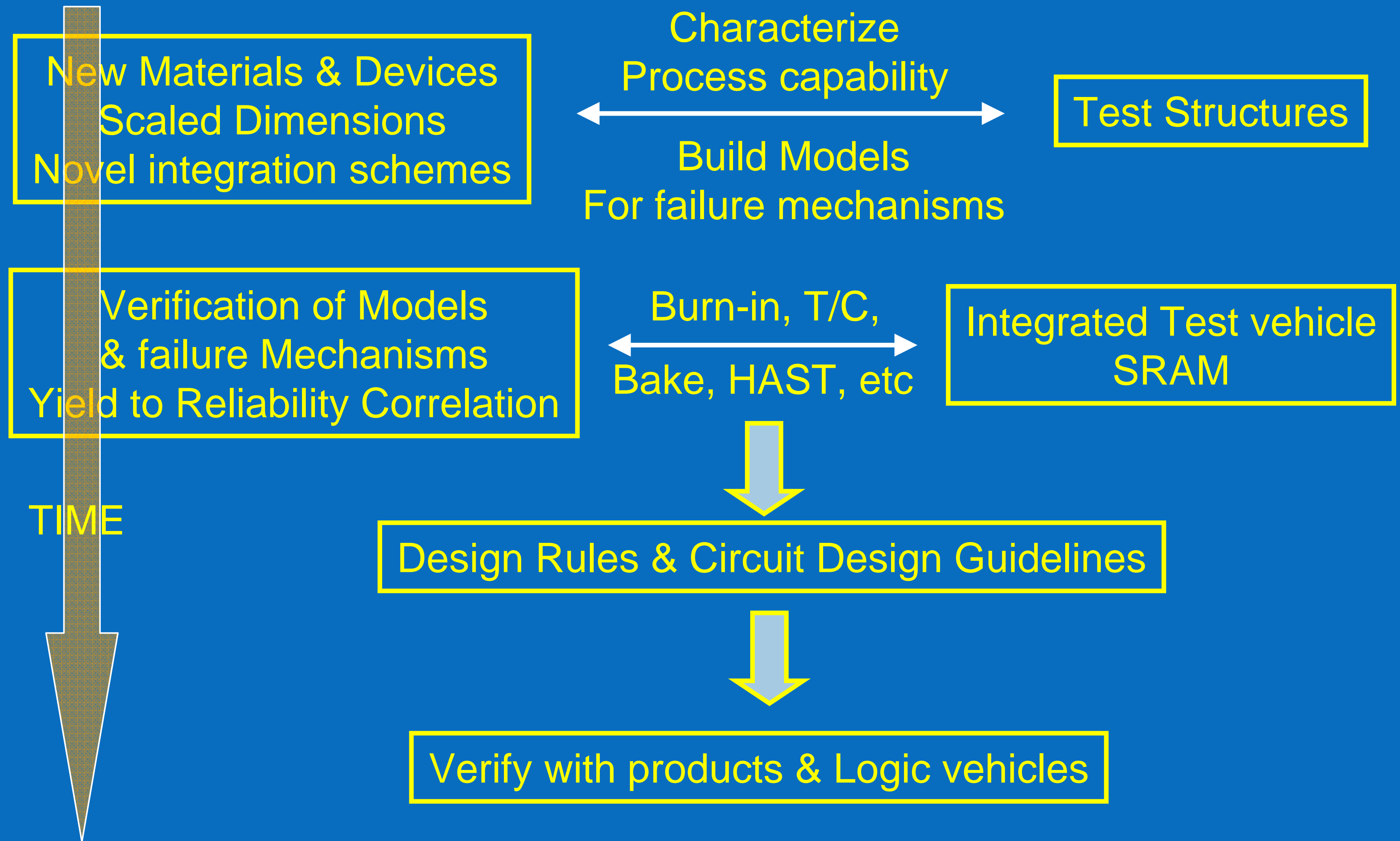
Process & product qualification Flows



Process & product qualification Flows Looking Forward

Low K dielectrics
Scaled Interconnect
Organic Flip-Chip packaging

Increased Thermo-mechanical and moisture risk

Aggressive scaling and novel transistors

Parametric degradation
Test Guardbands
Vmin & Fmax

Increased integration & functional content

Increased SEU risk
Fault tolerant circuits & architectures

Complex architectures
Multi-Core
System on a Chip

Increased Test complexity